CLAIMS

What is claimed is:

1. A semiconductor structure comprising:
a pad area; and
an active device of said semiconductor structure disposed below said pad area.

2. The semiconductor structure as recited in Claim 1 wherein said active component comprises a transistor.

3. The semiconductor structure as recited in Claim 1 wherein a component of said semiconductor structure performs a logic function.

4. The semiconductor structure as recited in Claim 1 wherein a component of said semiconductor structure performs a memory function.

5. The semiconductor structure as recited in Claim 1 wherein said active device comprises a first device, said semiconductor structure further comprising:
a non-pad area bounded at least in part by said pad area; and
a second device disposed within said non-pad area.

6. The semiconductor structure as recited in Claim 5 wherein said first and said second devices perform a similar function.

7. The semiconductor structure as recited in Claim 1 wherein said pad area comprises:
a substrate;
a first layer of metal disposed above said substrate wherein said active device is disposed below said first layer of metal;
a second layer of metal disposed above said first layer of metal.

8. The semiconductor structure as recited in Claim 7 further comprising:
a layer of dielectric disposed between said first metal layer and said second metal layer; and
a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer.

9. The semiconductor structure as recited in Claim 7 further comprising a subsequent layer of metal between said first and said second metal layers.

10. A pad area apparatus for a semiconductor structure comprising:
a substrate;

a first layer of metal disposed above said substrate;
a second layer of metal disposed above said first layer of metal; and
an active component wherein said active component is disposed within said substrate.

11. The pad area apparatus as recited in Claim 10 further comprising:
a layer of dielectric disposed between said first metal layer and said second metal layer; and
a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer.

12. The pad area apparatus as recited in Claim 10 further comprising a subsequent layer of metal between said first and said second metal layers.

13. A method for fabricating a semiconductor structure, comprising:
providing a pad area; and
disposing an active device of said semiconductor structure below said pad area.

14. The method as recited in Claim 13 wherein said active device comprises a transistor.

15. The method as recited in Claim 13 wherein a component of said semiconductor semiconductor structure performs a logic function.

16. The method as recited in Claim 13 wherein a component of said semiconductor semiconductor structure performs a memory function.

17. The method as recited in Claim 13 wherein said active device comprises a first device, and wherein said method further comprises:
providing a non-pad area bounded at least in part by said pad area; and
disposing a second device within said non-pad area.

18. The method as recited in Claim17 wherein said first and said second components perform a similar function.

19. The method as recited in Claim 13 wherein said providing a pad area comprises:
forming a substrate;
disposing said active device within said substrate;
disposing a first layer of metal above said substrate; and
disposing a second layer of metal above said first layer of metal.

20. The method as recited in Claim 19 further comprising:

disposing a layer of dielectric between said first metal layer and said second metal layer; and

disposing a via within said dielectric layer wherein said via electrically couples said first and said second metal layer.

21. The method as recited in Claim 19 further comprising disposing a subsequent layer of metal between said first and said second metal layers.